Empyrean Patron™

DATASHEET

High-performance and Accurate Power Integrity Verification

Benefits

Comprehensive analysis

- Including EMIR analysis, self-heating effect (SHE), multi-state EMIR, Chip Power Model (CPM) generation, and Failure-In-Time (FIT) calculations.

Fast and accurate

- Integrating with Empyrean ALPS® engine providing industrial-certified accuracy from block-level to large post-layout designs

Easy-to-use

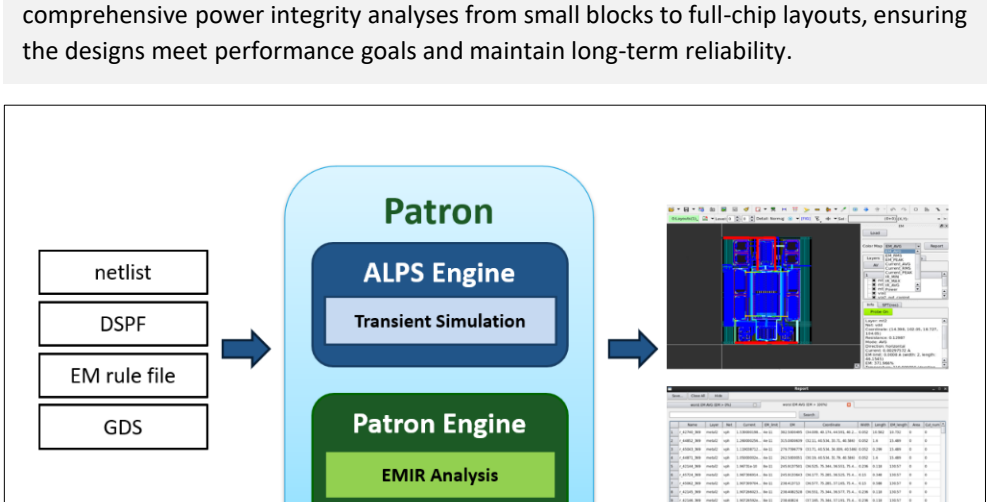
- Supporting intuitive Graphical User Interface (GUI) to help view and analyze results in the layout view.

Unmatched scalability

- Utilizing CPU-GPU architecture to ensure exceptional performance and scalability ensuring meeting aggressive time-to-market goals.

Moore's Law and Post-Moore's Law are driving the industry to integrate an increasing number of transistors into shrinking chips, resulting in higher current density. Consequently, the importance of electromigration and IR-drop (EMIR) analysis is increasing with the advancements in process technology and low-power designs. EMIR analysis is now essential even for the legacy technology process with rapidly increasing IoT and automotive electronic products. The demand for high reliability and support for power supply up to hundreds of volts introduces new verification requirements for analog ICs.

Empyrean Patron™ is a high-performance and accurate power integrity tool designed for transistor-level power and signal net electromigration (EM) analysis and power net IR-drop analysis for analog and mixed-signal designs. It enables designers to perform comprehensive power integrity analyses from small blocks to full-chip layouts, ensuring the designs meet performance goals and maintain long-term reliability.



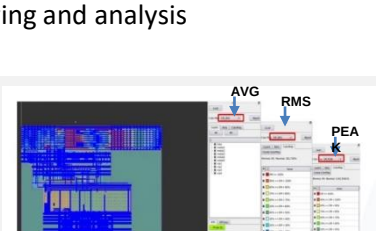
Empyrean Patron™ offers comprehensive capabilities, including EMIR analysis, self-heating effect (SHE), multi-state EMIR analysis, Chip Power Model (CPM) generation, and Failure-In-Time (FIT) calculations to help mitigate the effect of electromigration failures and ensure reliable circuitry.

A significant challenge of transistor-level dynamic EMIR analysis is the ability to simulate large post-layout circuits. Patron addresses this issue by integrating with the best-in-class SPICE simulator engine, Empyrean ALPS®, to ensure accurate simulation and analysis from block-level designs to large post-layout designs. Its proprietary Smart Matrix Solver (SMS) technology delivers a superior performance advantage in post-layout simulations. Additionally, it leverages the CPU-GPU technology to enable extensive scaling and parallelization, thereby delivering exceptional performance and scalability. This results in performance enhancement exceeding 10x compared to traditional CPU-based solutions.

Features

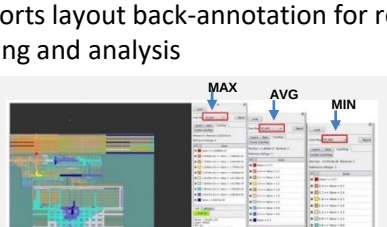
❖ Dynamic EM analysis

- Power net and signal net EM analysis
- Supports Average, RMS, and Peak modes
- Supports layout back-annotation for result viewing and analysis



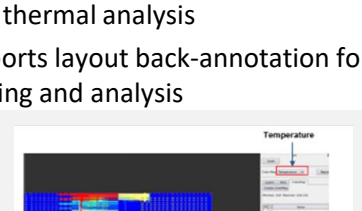
❖ Dynamic IR-drop analysis

- Power net IR-drop analysis
- Support Maximum, Average, and Minimum modes
- Supports layout back-annotation for result viewing and analysis



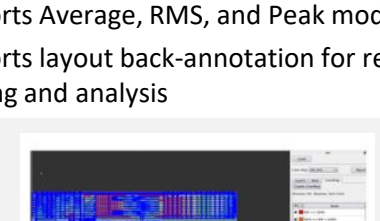
❖ Self-heating analysis

- Device and OD thermal
- Coupling thermal
- Path thermal analysis
- Supports layout back-annotation for result viewing and analysis



❖ Dynamic EM analysis with SHE

- Power net and signal net EM analysis with SHE
- Supports Average, RMS, and Peak modes
- Supports layout back-annotation for result viewing and analysis



Additional Features

❖ Multi-State EM analysis

- EM analysis of multiple states in one simulation

❖ Minimum resistor path

- Calculation of minimum resistance path from net to pins and back-annotate result into the layout view

❖ Chip Power Model Generation

- Effective creation of CPMs for power integrity verification

❖ Failure-In-Time calculations

- Predictive analysis of component lifespan and reliability