Empyrean Polas™

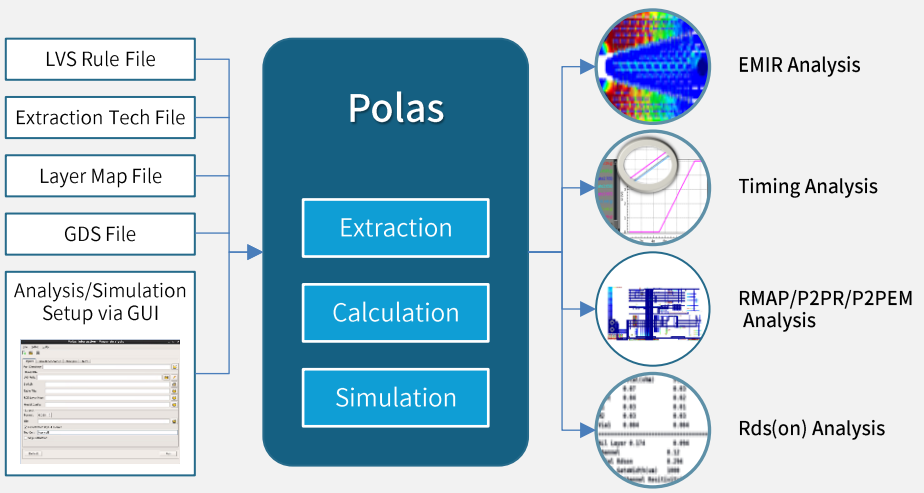
DATASHEET

Powerful Solution for Analyzing and Optimizing Power Devices

Benefits

- **Complete system for PMIC designs**
  Highly integrated system, including Extraction, Simulation, and Results Viewing and Analysis.
- **Comprehensive analysis**
  Including fast and accurate Rds(on) calculation, EMIR analysis, power device timing analysis, RMAP analysis, etc.
- **Efficient 3D field solver**
  Accurately handling special shapes and large areas of PMIC designs.
- **Intuitive GUI**
  Easy-to-use GUI to help set up and analyze results.
- **Sign-off solution**
  Adopted by many PMIC customers to tape out billions of chips.

Empyrean Polas™ stands as a vital tool for power IC designers, enhancing the reliability and yield of Power Management Integrated Circuit (PMIC) designs. Its advanced 3D field solvers extraction algorithm efficiently tackles the limitations of traditional RC extraction methods, adeptly managing the special shapes and large areas of power devices in PMIC designs. Serving as a comprehensive one-stop solution, Empyrean Polas™ empowers designers to ensure the quality of their designs, preempting unnecessary costly, and time-consuming re-spins.



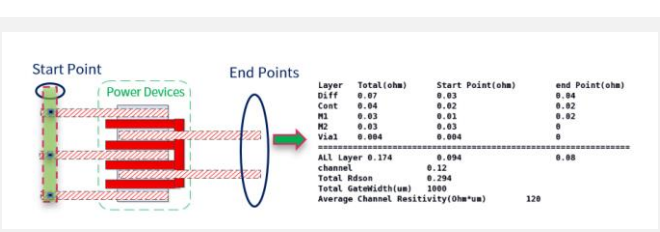
Empyrean Polas™ provides comprehensive capabilities such as fast and accurate Rds(on) calculation, Electromigration and IR-drop (EMIR) analysis, power device timing analysis, and cross-monitor/power-device EM analysis to analyze the performance and characteristics of power devices. It also supports RMAP/P2PEM/P2PR analysis allowing you to inspect the layout Power Distribution Network and critical signal paths such as the ESD network and differential clocks network.

In PMIC designs, the different loadings of different modules have impacts on the resistance distribution and current density distribution on the path. Accounting the scenarios with different loading reflects the more realistic network resistance and current density. RMAP is a layout resistance network analysis and mapping feature. P2PEM and P2PR allow multi-points to multi-points network resistance, voltage drop, current density inspection, and mapping features. Consequently, RMAP/P2PEM/P2PR analysis conducts a comprehensive assessment of the layout, encompassing both physical and electrical characteristics, empowering you with profound insights into the physical designs.

Features

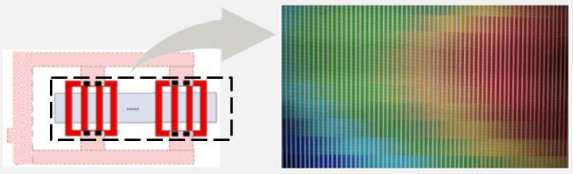
❖ Fast and accurate Rds(on) analysis

- Leveraging by SPICE circuit simulation technology to facilitate fast and accurate Rds(on) calculations to guide design and layout optimization.



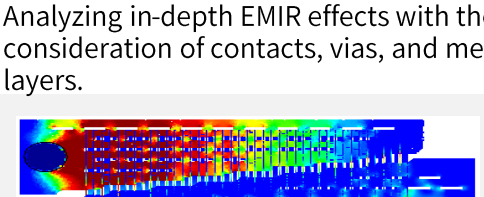
❖ Accurate timing analysis for power devices

- Analyzing the gate delay/rising/falling distribution of power MOSFETs using extraction and simulation engines.



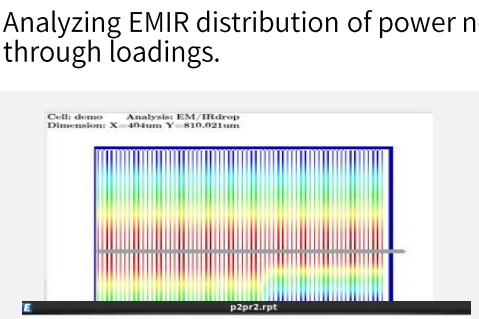
❖ Efficient EMIR analysis

- Analyzing in-depth EMIR effects with the consideration of contacts, vias, and metal layers.



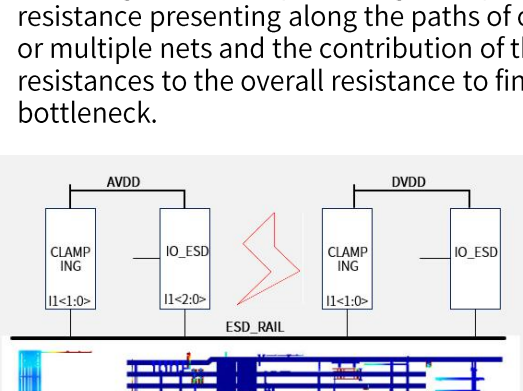
❖ Useful P2PEM/P2PR analysis

- Reporting effective resistance for critical paths.
- Analyzing EMIR distribution of power nets through loadings.



❖ Powerful RMAP analysis

- Providing a visual map showing the layout resistance presenting along the paths of one or multiple nets and the contribution of these resistances to the overall resistance to find the bottleneck.



❖ Effective Cross-monitoring

- Checking the shoot-through current when the high-side and low-side of power MOSFETs are simultaneously on to add dead-time if needed and prevent straight High-side/Low-side circuit.