GPU-Powered SPICE: The latest Breakthrough Technology for Analog Simulation

Chen Zhao, Application Engineering Manager,

Empyrean Software

Introduction

Recently, one customer shared his experience of benefiting from Moore's Law as an analog designer. They replaced their old servers with those using latest CPUs. He found that there's an average of ~2X speedup on his simulations with new servers. This improvement all comes from the contribution of CPU's hardware since he's using the same SPICE with the same settings. Following Moore's Law, CPU's performance improvement is predictable and yet slow. It takes years of waiting for designers to benefit for simulation. Therefore, analog designers tend to look for faster SPICE instead. SPICE developers have put lots of effort to improve speed. There are several technologies to shorten simulation time:

- Speedup from SPICE algorithm relaxation
- Speedup from RC reduction
- Speedup from parallelization

For a long time, SPICE run on one single CPU. With this hard limit of computing resource, one approach to run simulation faster is through reducing the computation complexity of algorithms. Fast SPICE is the product of this idea. It utilizes approaches such as event-driven simulation, model reduction and multi-rate simulation to run faster. However, it comes with the cost of unpredictable accuracy, especially in deep sub-micron processes.

RC reduction is another way to reduce computation complexity. Time Constant Equilibration Reduction (TICER) is a widely used RC reduction method. Typically, it can trim 80% or even 90% of parasitic RCs. Circuit design in advanced nodes may have 1:10 to 1:100 of transistors to parasitic RCs ratio. If more than 90% of RC in a circuit are trimmed, the simulation will run faster. Still, it comes with cost of accuracy loss, especially in deep sub-micron processes and high frequency designs.

Then parallel SPICE became available more than ten years ago when multi-core CPU was widely adopted. Parallelization easily provides several folds of computing resource to SPICE algorithm, thus making simulation runs 3~5X faster with 8-CPU configuration compared with single CPU. Even better, there's no loss of accuracy with parallelization. Typically, a parallel SPICE simulation job consists of several major tasks. Netlist parsing and building database are usually done sequentially. Then the simulator can use parallel processing techniques, such as multi-core and multi-threading, to speed up tasks for calculating DC operating point and transient analysis.

Design Challenges in Advanced Process

While designers can enjoy the benefit of Moore' s Law to run simulation faster, such as more available cores and higher single core performance of CPU, the same law also causes more trouble. Due to the shrinking geometry and complicated 3D structure, current advanced process brings significantly more complex models, parasitic RCs and corners. These all contribute to a longer simulation time than previous planar technologies. Take a digital frequency divider designed in 7nm technology for instance, it only takes 10 mins for schematic simulation. But it will take more than 10 hours when running with extracted netlist. The 60X time difference comes from number of parasitic RCs being almost 100X more than transistors. For the same circuit, when it was designed with 16nm process, it only takes 2 hours when running with extracted netlist. That means, designer need to spend 6X the time with the new process. And this is for one single run. Let' s say you have 5 process corners, 3 supply voltages, 3 temperatures and 2 RC corners, you will need to run 90 combinations to verify the circuit. Given that, with almost fixed tape-out schedule and time-to-market, designers need a solution to address their verification challenges.

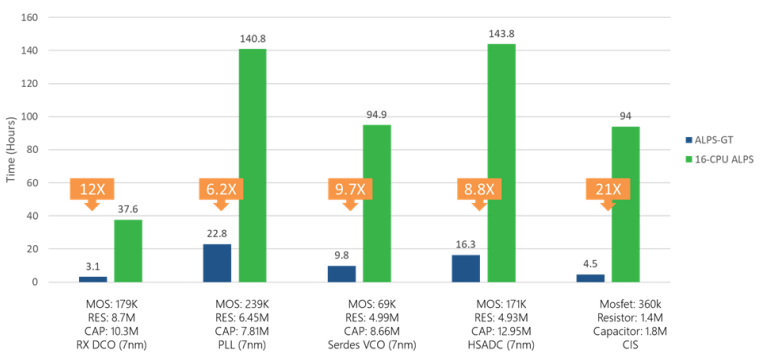
Empyrean ALPS-GT™

Empyrean ALPS-GT™, the first commercial GPU-accelerated circuit simulator, provides up to 50X performance gain while maintaining great correlation to your golden results. Using GPU for acceleration is the latest breakthrough in parallel SPICE. With thousands of cores available in GPU, Empyrean ALPS-GT™ can simulate designs much faster than traditional CPU-based parallel SPICE. Even better, using GPU for acceleration will not introduce any accuracy issue, since the engine will still solve the same matrix only with much more available computation resource compared with traditional CPU-based parallel SPICE.

Using Empyrean ALPS-GT™ for Circuit Verification

Empyrean ALPS-GT™ was developed to address circuit designer' s headache of balancing accuracy and runtime. Especially, when running high accuracy circuit simulation in advanced process nodes and with millions of parasitic RCs. And because of the nature of GPU parallelization, the larger the design and the more parasitic RCs, the better speedup Empyrean ALPS-GT™ will provide. Empyrean ALPS-GT™ is compatible with industry' s golden netlist syntax, thus making it hassle-free adoption.

Running parallel SPICE with 16 CPUs provides the most practical performance for a circuit designer. Empyrean ALPS-GTTM can provide additional 5-10X speedup over 16-CPU Empyrean ALPS without any accuracy loss.



ADC (Analog to Digital Converter) is an important building block in many SoCs. That means an ADC must be designed in advanced process along with the digital parts in an SoC, where a huge number of parasitic RC elements must be taken into consideration. To understand how accurate an ADC is, designers must run high accuracy simulation to check specifications such as noise, effective number of bits (ENOB) and power. And running high accuracy simulation in advance process nodes comes with long verification time. Empyrean ALPS-GT™ can provide significant improvement on productivity to reduce verification time. Here's an example of ADC verification in FinFET technology. The benchmark is between Empyrean ALPS-GT™ and other mainstream SPICEs.

	Reference Spec	Tool-1	Tool-2	ALPS-GT
ENOB	6.85 – 7.05 bit	7.02 bit	6.96 bit	7.03 bit
Current	523uA +/- 2%	525.2 uA	534.1 uA	522.9 uA
Run Time	-	65.8 hours	54 hours	2.8 hours
Speedup	-	23.5X	19.3X	-

Conclusion

Empyrean ALPS-GT™ greatly improves simulation time especially in advance process nodes and high accuracy designs. With 10X+ acceleration and the same accuracy, Empyrean ALPS-GT™ can greatly boost your productivity by:

- Shortening design cycles with much shorter simulations
- Enabling faster time to tape-out and eventually, time to market.

It also helps you improve silicon success:

- Covers more PVT corners in a fixed design schedule
- Enables new types of simulation that were previously impossible such as fully extracted, top-level simulation.

To learn more about user's feedback on Empyrean ALPS-GT™, please go to deepchip.com for their 2019 best of DAC report: http://www.deepchip.com/items/dac19-02c.html

Sales Contacts

Headquarters
Empyrean Software

2F Building A, Wang Jing Hi-Tech Park,
No.2 Lizezhonger Road, Chaoyang
District, Beijing, 100102, P. R. China
TEL: +86-10-84776888
FAX: +86-10-84776889
Web: www.empyrean-tech.com
EMAIL: info@empyrean-tech.com

USA
Empyrean Software
4030 Moorpark Ave, Suite 109, San Jose,
CA 95117
TEL: +1 (669) 230-5019
www.empyrean-tech.com
E-mail: info@empyrean-tech.com

Korea
linkGlobal21
#301, 81, Hyeonam-ro, Suji-gu,
Yongin-si, Gyeonggi-do,Korea
Tel: +82-70-5138-0700
www.lg21.net/
E-mail: eda@linkglobal21.com

Singapore
MEDs Technologies Pte.Ltd.
5012, Ang Mo Kio Avenue 5 #04-01
Techplace II, Singapore 569876
Tel: +65 6453 8313
Fax: +65 6453 7738
www.meds-tech.com

Japan
Xloud Inc.
Dojima Axis Building 4F,
2-2-28 Dojimahama, Kita-ku,
Osaka, 530-0004 Japan
Tel: +81-6-6123-7784
https://xloud.co.jp
E-mail: eda_sales@Xloud.co.jp